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BIRCH STEWART KOLASCH & BIRCH
PO BOX 747
FALLS CHURCH, VA 22040-0747

EXAMINER	
KALAM, ABUL	

ART UNIT	PAPER NUMBER
2814	

NOTIFICATION DATE	DELIVERY MODE
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Please find below and/or attached an Office communication concerning this application or proceeding.

The time period for reply, if any, is set in the attached communication.

Notice of the Office communication was sent electronically on above-indicated "Notification Date" to the following e-mail address(es):

mailroom@bskb.com

Office Action Summary	Application No.	Applicant(s)	
	10/526,009	FUJII ET AL.	
	Examiner	Art Unit	
	Abul Kalam	2814	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE *3* MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *23 December 2009*.

2a)☒ This action is **FINAL**. 2b)☐ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-6,9,10,26-29 and 34-40* is/are pending in the application.

4a) Of the above claim(s) *5,6,9 and 36-38* is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-4,10,26-29,34,35,38 and 40* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☐ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____ .
5) ☐ Notice of Informal Patent Application
6) ☐ Other: _____.

Claim Rejections - 35 USC § 103

The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (e) the invention was described in (1) an application for patent, published under section 122(b), by another filed in the United States before the invention by the applicant for patent or (2) a patent granted on an application for patent by another filed in the United States before the invention by the applicant for patent, except that an international application filed under the treaty defined in section 351(a) shall have the effects for purposes of this subsection of an application filed in the United States only if the international application designated the United States and was published under Article 21(2) of such treaty in the English language.

1. **Claims 1, 10, 34, 39 and 40** are rejected under 35 U.S.C. 103(a) as being unpatentable over Wong et al. (US 2004/0002225; hereinafter, Wong).

With respect to **claim 1**, Wong teaches a TFT array substrate **(Fig. 7)**, comprising:

a thin film transistor section **(¶ [0045])** in which a gate electrode **(724, Fig. 7)** is formed on a substrate **(708)**, and

a semiconductor layer **(732, Fig. 7)** is formed by etching a semiconductor film after a mask material is dropped onto the semiconductor film **(¶ [0049])** and is formed on the gate electrode **(724)** separated by a gate insulation layer **(728, ¶ [0048])**, wherein the semiconductor layer **(732)** having dimensions along a periphery defined as a result of being formed by dropping droplets of the mask material **(¶ [0044]-[0049], [0020]-[0030])**. Thus, Wong teaches all the limitations of the claim with the exception of explicitly disclosing "dropping a single droplet of the mask material." However, note the phrase, "dropping a single droplet of the mask material" is drawn to a "product by process" limitation. It has been held that a product by process claim is directed to the

product per se, no matter how actually made. *In re Thorpe et al.,* 227 USPQ 964, (CAFC, 1985) and the related case law cited therein make it clear that it is the final product per se which must be determined in a "product by process" claim, and not the patentability of the process, and that, as here, an old or obvious product produced by a new method is not patentable as a product, whether claimed in "product by process" claims or not. As stated in Thorpe:

> Even though product-by-process claims are limited by and defined by the process, determination of patentability is based on the product itself. *In re Brown*, 459 F.2d 531, 535, 173 USPQ 685, 688 (CCPA 1972); *In re Pilkington,* 411 F.2d 1345, 1348, 162 USPQ 145, 147 (CCPA 1969); *Buono v. Yankee Maid Dress Corp.*, 77 F.2d 274, 279, 26 USPQ 57, 61 (2d. Cir. 1935);

Furthermore, Wong discloses that the size of the droplets of the mask material may be adjusted depending on the desired size of the features **(¶ [0027])**, and thus, it would have been obvious for Wong to form a semiconductor layer having dimensions which are formed by a single droplet. Also, note the Applicant has not disclosed any criticality or unpredictable results to the claimed invention from using a single droplet of mask material rather than the multiple droplets taught by Wong.

Regarding **claim 10**, Wong discloses that liquid crystal displays comprising a TFT substrate was well known and conventional at the time of the invention **(¶ [0001])**. Furthermore, it has been held that a preamble is denied the effect of a limitation where the claim following the preamble is a self-contained description of the structure not depending for completeness upon the introductory clause. *Kropa v. Robie,* 88 USPQ 478 (CCPA 1951).

Regarding **claim 34**, Wong teaches an electronic device including the TFT array substrate as set forth in claim 1 **(¶ [0045])**. Regarding the limitation of an electronic

device, it has been held that a preamble is denied the effect of a limitation where the claim following the preamble is a self-contained description of the structure not depending for completeness upon the introductory clause. *Kropa v. Robie,* 88 USPQ 478 (CCPA 1951).

Regarding **claims 39 and 40**, note that the limitation of "a substantially circular shape" having “a diameter of approximately 30 μm” for the semiconductor layer, would have been obvious to one of ordinary skill in the art because, without evidence of criticality for the particular shape or dimension, a change in the shape or dimensions of a feature is generally recognized as being within the level of ordinary skill in the art. See *In re Rose*, 220 F.2d, 105 USPQ 237 (CCPA 1955) and *In re Dailey*, 357 F.2d 669, 149 USPQ 47 (CCPA 1966). Furthermore, it has been held that where the only difference between the prior art and the claims was a recitation of relative dimensions of the claimed device, and a device having the claimed relative dimension would not perform differently than the prior art device, the claimed device was not patentably distinct from the prior art device. See *Gardner v. TEC Systems, Inc.*, 725 F.2d 1338, 220 USPQ 777 (Fed. Cir. 1984), *cert. denied*, 469 U.S. 830, 225 USPQ 232 (1984).

2. **Claims 2-4** are rejected under 35 U.S.C. 103(a) as being unpatentable over Wong (cited above) in view of Kasahara et al. (US 6,822,701; hereinafter, Kasahara).

With respect to **claim 2**, Wong discloses all the limitations of claim, as set forth above in claim 1, including wherein the gate electrode **(724, Fig. 7)** in the thin film transistor section is a branch electrode which is branched out of a main line of the gate

electrode **(¶ [0045]: "bottom gate electrode of the TFT")**. However, Wong does not explicitly disclose wherein the branch electrode has an open end protruded from an area for the semiconductor layer.

However, Kasahara discloses a thin film transistor array **(Fig. 3)** wherein the gate electrode **(220)** in the TFT section **(24)** is branch electrode that has an open end **(Fig. 3, "e")** protruded from an area **(224A/224B)** of the semiconductor layer **(223, Fig. 2)**.

Regarding **claim 3,** Kasahara also teaches wherein the branch electrode is arranged so that a portion protruded **(Fig. 3, "e")** from the area for the semiconductor layer is smaller in width than a portion confined within the area **(224A/224B)** for the semiconductor layer.

Regarding **claim 4,** Kasahara also teaches wherein the thin film transistor section further includes a source electrode and a drain electrode **(221 and 222, Fig. 2)** on the semiconductor layer **(223)**, and a channel section is formed between the source and drain electrodes (a channel is inherently formed between the source and drain), and the portion of the branch electrode **(Fig. 3, "e")** protruded from the area for the semiconductor layer is formed in contact with one of the source and drain electrodes **(col. 14, lns. 31-40)**.

Therefore, it would have been obvious to one of ordinary skill in the art at the time of the invention, to combine the teaching of Kasahara and Wong, to form a thin film transistor array wherein the gate electrode comprises a branch electrode with a protruded portion, for the purpose of improving the process of repairing defective pixels in a display device **(col. 16, lns. 1-9)**.

3. **Claims 26-29 and 35** are rejected under 35 U.S.C. 103(a) as being unpatentable over Yi et al. (US 6,909,477; hereinafter, Yi) in view of Wong (cited above).

With respect to **claim 26,** Yi discloses a thin film transistor array substrate **(30, Fig. 3B)**, comprising:

a thin film transistor array section **(Fig. 3A and 3B)** in which a gate electrode **(32, Fig. 3B)** is formed on a substrate **(30)**, and in which a semiconductor layer **(36)** and a conductor layer **(38)** are formed on the gate electrode **(32)** separated by a gate insulation layer **(34)**;

wherein the conductor layer **(38, Fig. 3B)** is formed in contact with the semiconductor layer **(36)** and one of source and drain electrodes **(40 and 42)** of the thin film transistor section, wherein the conductor layer **(38)** and the semiconductor layer **(36)** having substantially the same dimensions along their respective periphery **(Figs. 3A, 3B and 4B; col. 5, lines 10-16)**.

Thus, Yi teaches all the limitations of the claim with the exception of disclosing wherein the semiconductor layer is formed by etching a semiconductor film after a mask material is dropped onto the semiconductor film; and wherein the conductor layer has a portion formed by dropping a droplet; and wherein the conductor layer and the semiconductor layer have substantially the same dimensions along their periphery as a result of being formed by dropping a droplet.

However, Wong teaches a TFT array substrate **(FIG. 7)** wherein a semiconductor layer **(732, Fig. 7)** is formed by etching a semiconductor film after a mask material is dropped onto the semiconductor film **(¶ [0049])**; wherein the semiconductor layer **(732)**

having dimensions along a periphery defined as a result of being formed by dropping droplets of the mask material; and wherein a conductor **(744)** has a portion formed by dropping a droplet **(¶ [0045]-[0049], [0020]-[0030])**.

Therefore, it would have been obvious to one of ordinary skill in the art at the time of the invention to incorporate the teaching of Wong into the invention of Yi, thereby forming the conductor layer and the semiconductor layer having substantially the same dimensions along the periphery by using printed masks formed by dropping a droplet, in place of conventional photolithography, for the disclosed purpose of reducing the size of critical features in thin film transistors.

Regarding **claim 27,** conductor layers such as Mo, W, Ag, Ta, Ti, and ITO are well known and conventional, and thus, would have been obvious to one of ordinary skill in the art at the time of the invention.

Regarding **claim 28,** Yi discloses wherein the source and drain electrodes are made of Al **(col. 5, lines 20-22)**.

Regarding **claim 29,** Yi discloses a liquid crystal display device **(Fig. 3A)** including the TFT array substrate as set forth in claim 26.

Regarding claim 35, Yi discloses an electronic device **(Fig. 3A)** including the TFT array substrate as set forth in claim 26.

Response to Arguments

4. Applicant's arguments filed on December 23, 2009, have been fully considered but are not persuasive.

Regarding claim 1, Applicant argues that Wong does not teach semiconductor layer 732 resulting form dropping droplets of mask material:

> "Forming of semiconductor layer (732) is described with respect to steps 628, 632, 636, and 640 of Fig. 6, at paras. 0048 and 0049 of Wong. In paragraph 0049, Wong discloses that an island structure is formed by depositing an etch mask 740 over a top dielectric layer, then etching the dielectric and semiconductor stack. The printed pattern is then removed to define the island features.
>
> However, Wong does not disclose that etch mask 740 is formed by applying droplets, which the Examiner has assumed.
>
> To the contrary, Wong discloses use of droplets with respect to forming of "fine features." In particular, Wong is directed to forming fine features (i.e., features having width that is less than 50 micrometers, as defined in para. 0032) at the spaces between patterns that have been formed by droplets. For example, as can be seen in Fig. 7, electrode 724 is formed at space 716 between patterns 712 in Fig. 7(a) after the patterns are removed.
>
> Applicants submit that Wong does not disclose semiconductor layer (732) having dimensions along a periphery defined as a result of being formed by dropping droplets of the mask material, e.g., 740."

The argument is not persuasive. As admitted by the applicant, Wong discloses that etch mask 740 is a printed pattern which is used to define the island features, including the semiconductor active layer (¶ [0049]). It is implicit that the printed patterns of Wong's invention are formed by dropping droplets of mask material (¶ [0044]), and thus, the dimensions of the active layer along a periphery are defined as result of being formed by dropping droplets of the mask material. Furthermore, Wong states: "The describe patterning process may be repeated on subsequently deposited layers, composed of bottom dielectric, semiconductor and top dielectric layer over entire substrate surface to form multiple TFTs (¶ [0048])." Thus, the patterning process described in paras. [0046]-[0048] in which an ink jet printing process is used (¶ [0046]), is also applicable to the semiconductor active layer.

As admitted by the applicant, Wong is directed to forming fine features at the spaces between patterns that been formed by dropping droplets, and thus, it is implicit that the droplets of the mask material determine the dimensions of the semiconductor layer, since the spacing between the droplets is inherently dependent on the size and positioning of the droplets.

Applicant also argues that Wong teaches away from using a single droplet. The argument is not persuasive. As stated in the Office Action, the phrase, "dropping a single droplet of the mask material" is drawn to a "product by process" limitation. It has been held that a product by process claim is directed to the product per se, no matter how actually made. Thus, it is dimensions of the semiconductor layer which is given consideration and is patentable, and not the process by which the semiconductor layer is formed. Applicant's argument that Wong teaches away from determining feature size based on droplet size is not found persuasive, since Wong clearly states:

> "As each drop is printed, a feedback system may be used to assure droplets of proper size. An imaging system, such as camera 122, may be used to monitor droplet size. When smaller features are to be printed, or the droplet size otherwise reduced, a temperature control circuit 123 lowers the temperature of a surface of substrate 120. The lower temperature increases the quench rate resulting in rapid solidification of the phase change patterning material upon contact with substrate 120. When larger droplets are needed, usually for merging droplets in larger features, temperature control circuit 123 raises the temperature of substrate 120 (¶ [0027])."

Furthermore, as stated above, the spacing between the droplets of mask material, which is used to define the "fine features" such as the semiconductor active layer, is inherently dependent on both the droplet size and the positioning of the droplets. Therefore, it would have been obvious for Wong to form a semiconductor

layer having dimensions along a periphery defined as a result of being formed by dropping a single droplet of the mask material, since Wong clearly states that the size of the droplets can be adjusted depending the size of the features, as underlined in paragraph [0027] above.

Applicant also argues that “a criticality of forming the semiconductor layer of a single droplet is to reduce the amount of time taken to manufacture the semiconductor layer and to extend the life of the ink jet head.” The argument is not persuasive. Note, the invention is directed to a device, and applicant's statement of criticality is directed to the process used to form the device, rather than the claimed invention itself. Applicant has not shown that the use of a “single droplet," as opposed to multiple droplets, is critical to claimed device or the dimensions of the claimed semiconductor layer. Furthermore, note that applicant states in the specification: “Though the resist layer 67 of this embodiment is formed by a single droplet with a pattern forming equipment, the resist layer 67 may also be formed by plural droplets (pg. 35, lines 8-10)." Thus, it is clear that the limitation of "a single droplet" is not critical to the claimed invention.

Regarding claim 26, Applicant argues:

> “Applicant submits that in addition to the differences over Wong as in claim 1, neither Wong nor Yi disclose a final end product in which each of the conductor layer and semiconductor layer take on a shape resulting from having been formed by dropping a droplet."

The argument is not persuasive. First, note that the claim does not recite “a final end product in which each of the conductor layer and semiconductor layer take on a shape resulting from having been formed by dropping a droplet," as argued by the

applicant. Instead, the claim recites the conductor layer and the semiconductor layer having substantially the same dimensions along respective periphery as a result of being formed by dropping a droplet. These limitations are obvious due to the teachings of Wong, as stated above in the Office Action:

> "Wong teaches a TFT array substrate **(FIG. 7)** wherein a semiconductor layer **(732, Fig. 7)** is formed by etching a semiconductor film after a mask material is dropped onto the semiconductor film **(¶ [0049])**; wherein the semiconductor layer **(732)** having dimensions along a periphery defined as a result of being formed by dropping droplets of the mask material; and wherein a conductor **(744)** has a portion formed by dropping a droplet **(¶ [0045]-[0049], [0020]-[0030])**.
>
> Therefore, it would have been obvious to one of ordinary skill in the art at the time of the invention to incorporate the teaching of Wong into the invention of Yi, thereby forming the conductor layer and the semiconductor layer having substantially the same dimensions along the periphery by using printed masks formed by dropping a droplet, in place of conventional photolithography, for the disclosed purpose of reducing the size of critical features in thin film transistors."

Conclusion

5. **THIS ACTION IS MADE FINAL.** Applicant is reminded of the extension of time policy as set forth in 37 CFR 1.136(a).

A shortened statutory period for reply to this final action is set to expire THREE MONTHS from the mailing date of this action. In the event a first reply is filed within TWO MONTHS of the mailing date of this final action and the advisory action is not mailed until after the end of the THREE-MONTH shortened statutory period, then the shortened statutory period will expire on the date the advisory action is mailed, and any extension fee pursuant to 37 CFR 1.136(a) will be calculated from the mailing date of the advisory action. In no event, however, will the statutory period for reply expire later than SIX MONTHS from the mailing date of this final action.

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Abul Kalam whose telephone number is (571)272-8346.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Wael M. Fahmy can be reached on 571-272-1705. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free). If you would like assistance from a USPTO Customer Service Representative or access to the automated information system, call 800-786-9199 (IN USA OR CANADA) or 571-272-1000.

/A. K./
Examiner, Art Unit 2814

/Wael M Fahmy/
Supervisory Patent Examiner, Art Unit 2814